Low Power Flight Experiment: Flight-Qualifying Sub-0.25-µm Fully Depleted SOI CMOS Technology

Deep Space 1 Technology Validation Symposium

9 February 2000

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www.LL.mit.edu/AST

Acknowledgements

Eric Holmberg - LPE Cognizant Engineer

Kirk Fleming - LPE Post Launch Engineer

Pete Daniels - MIT/LL (SOI Packaging)

MIT/LL Microelectronics Laboratory Staff- SOI Fab

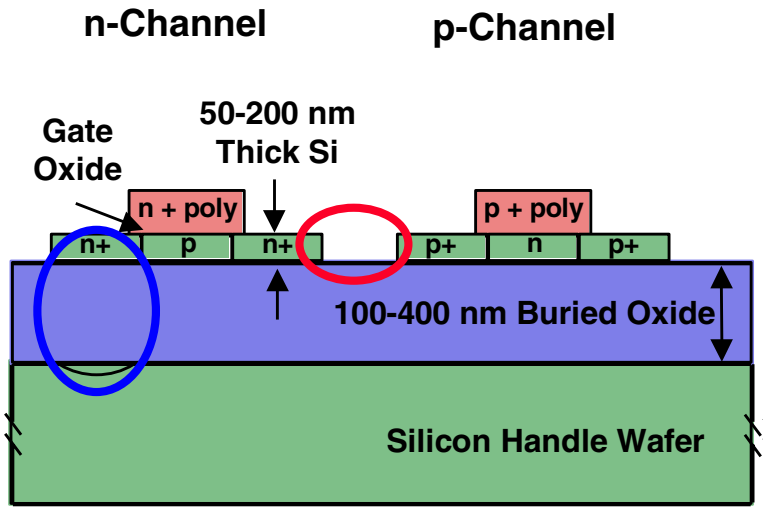
Leon Alkalai and Chuck Minning - LPE Program Management

Outline

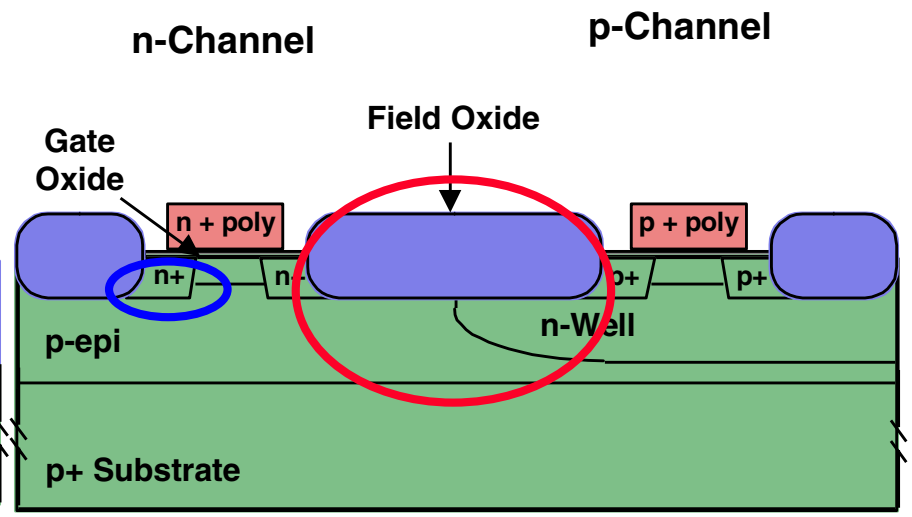
- Sub-0.25-µm fully depleted SOI CMOS process technology
- Low Power Experiment overview
  - Test system design
  - Flight experiment results
- The future of the technology
- Summary

Advantages of SOI CMOS
Reduced Device and Circuit Capacitance

SOI CMOS Cross Section

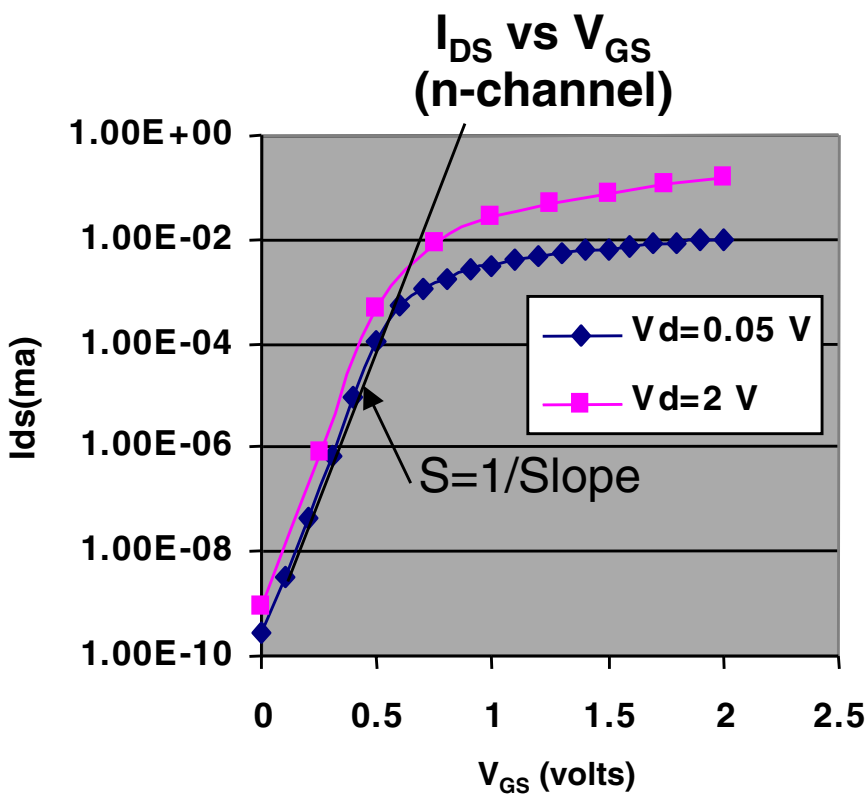


n-Well Bulk CMOS Cross Section



- **Advantages for both PDSOI and FDSOI**
  - ⇒ – **Device spacing at near minimum lithography limit for reduced interconnect wiring capacitance**
  - ⇒ – **Source and Drain regions are fully diffused to buried oxide interface for reduced junction capacitance**

Enhanced Subthreshold Swing (S)
FDSOI's Performance Advantage



$$S \approx \frac{kT}{q} \ln 10 \cdot \frac{C_{ox} + C_D}{C_{ox}}$$

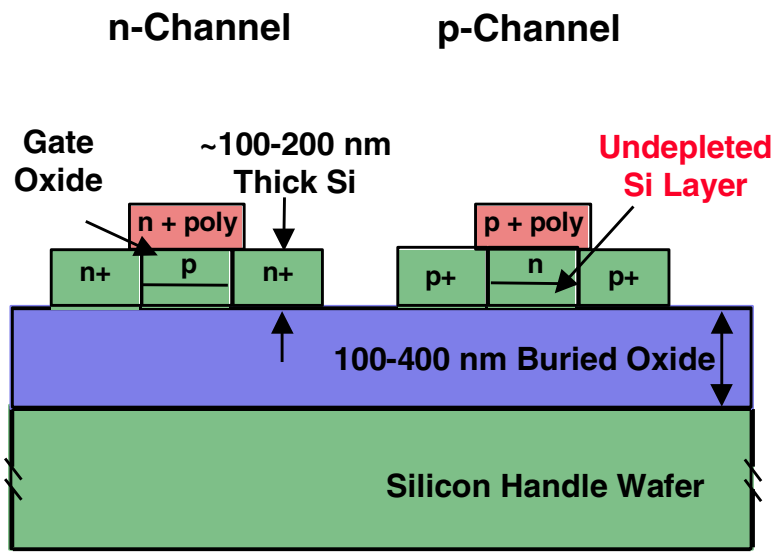
For bulk and PDSOI:
1/S ~ 85-90 mV/decade

For FDSOI:
1/S ~ 65-70 mV/decade

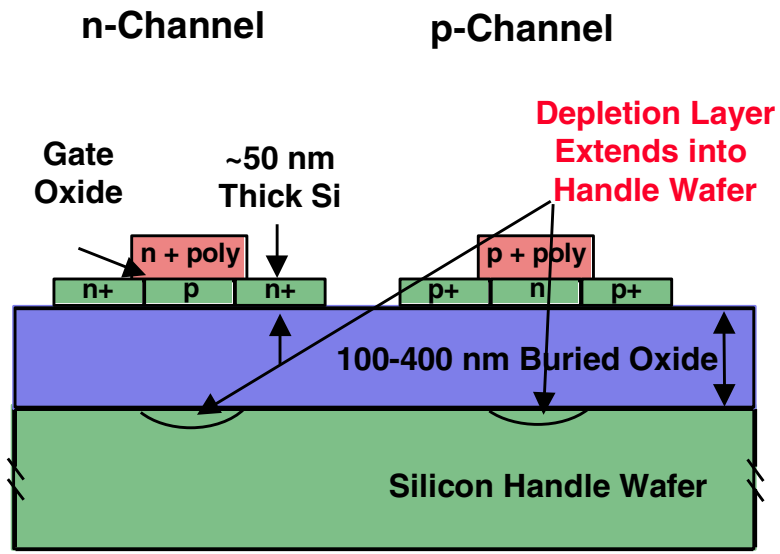
Ideal at room temperature:
1/S ~ 60 mV/decade

Enhanced Subthreshold Swing (S)
FDSOI's Performance Advantage (cont.)

Partially Depleted Cross Section



Fully Depleted Cross Section



$$S \approx \frac{kT}{q} \ln 10 \cdot \frac{C_{ox} + C_D}{C_{ox}}$$

$$f_T \approx \frac{g_m}{2\pi (C_{gs} + C_D)}$$

- The depletion capacitance C_D for the FDSOI transistor is reduced by the buried oxide thickness

Motivation for SOI

Reduced Power and Enhanced Performance of FDSOI CMOS

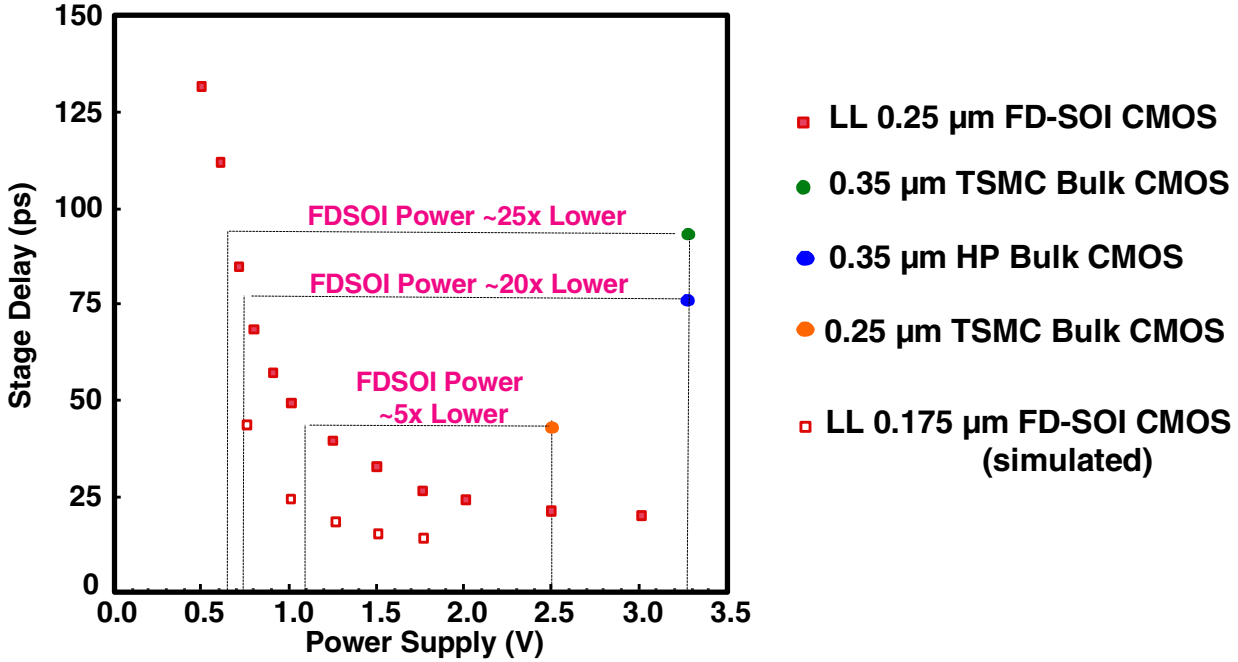
Digital CMOS Power: $P = CV^2f$

- Key to lower power operation - lower V
  - In order to maintain transistor current drive, lower power supply voltage requires lower threshold voltages
  - Improved subthreshold slope of FDSOI transistors allows lower threshold voltages
- SOI also offers lower capacitance (C)
  - Increased device packing density reduces interconnect wiring C
  - Transistor source and drain parasitic C also reduced.

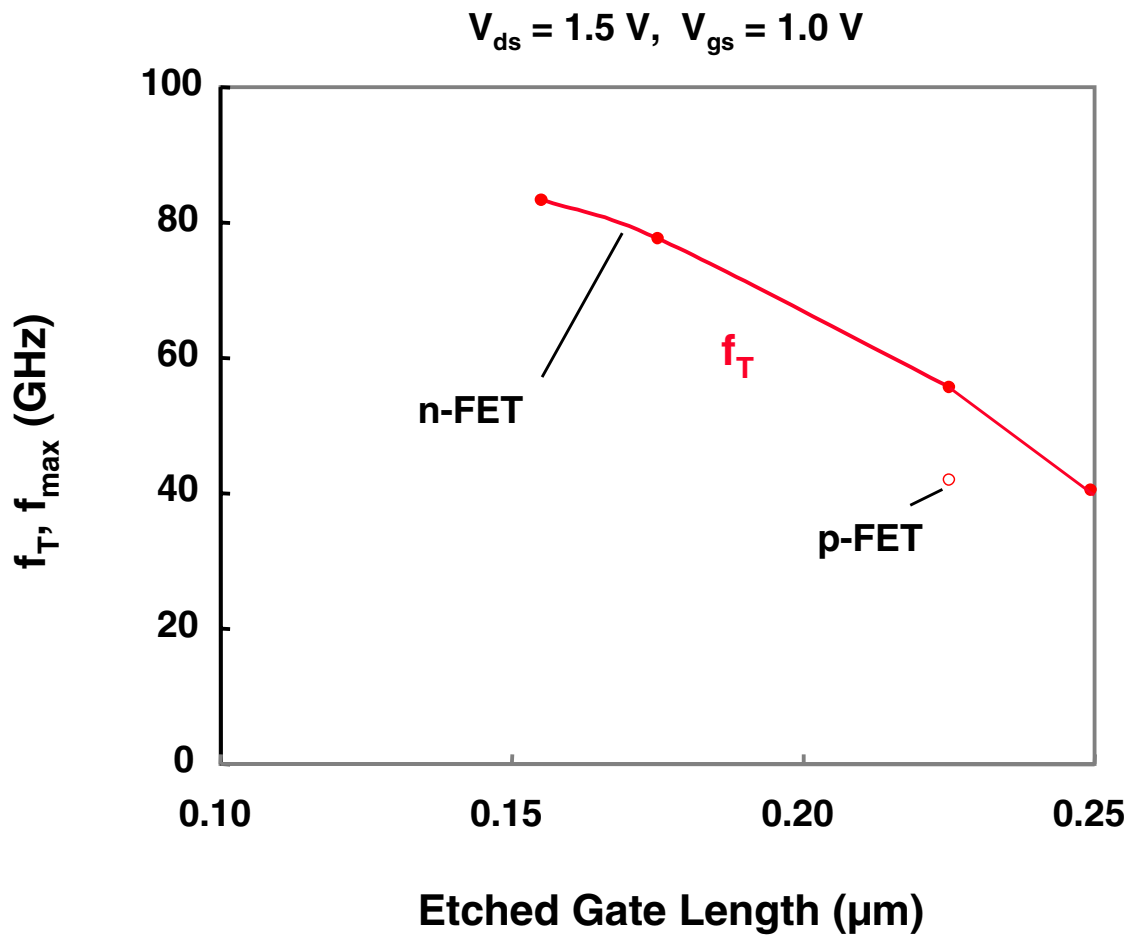
Motivation for SOI (cont.)

Reduced Power and Enhanced Performance of FDSOI CMOS

Ring Oscillator Stage Delay
(Fanout = 1)



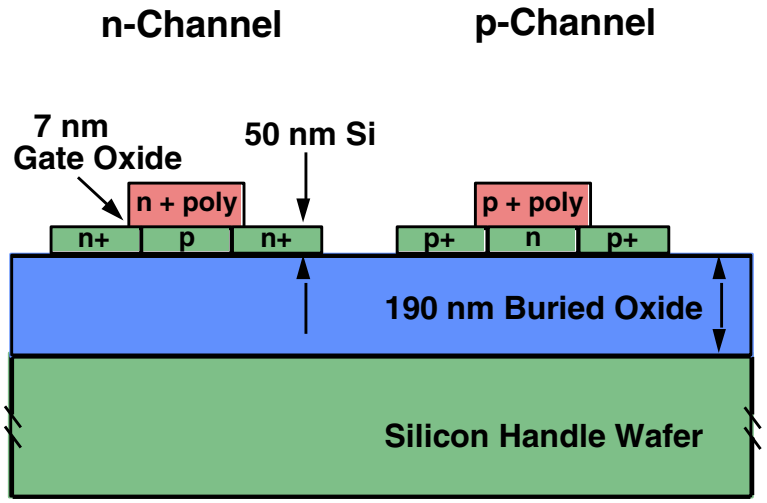
FDSOI f_T as a Function of Gate Length



Process Highlights

- 0.25 µm fully depleted silicon-on-insulator (FDSOI) process
- 50 nm thick active silicon layer with mesa isolation
- 0.25 µm drawn, dual-doped polysilicon gates
- 25 nm Ti-capped cobalt salicide process
- Aluminum damascene stacked contact and via plugs
- Fully planar 3-level metal interconnect

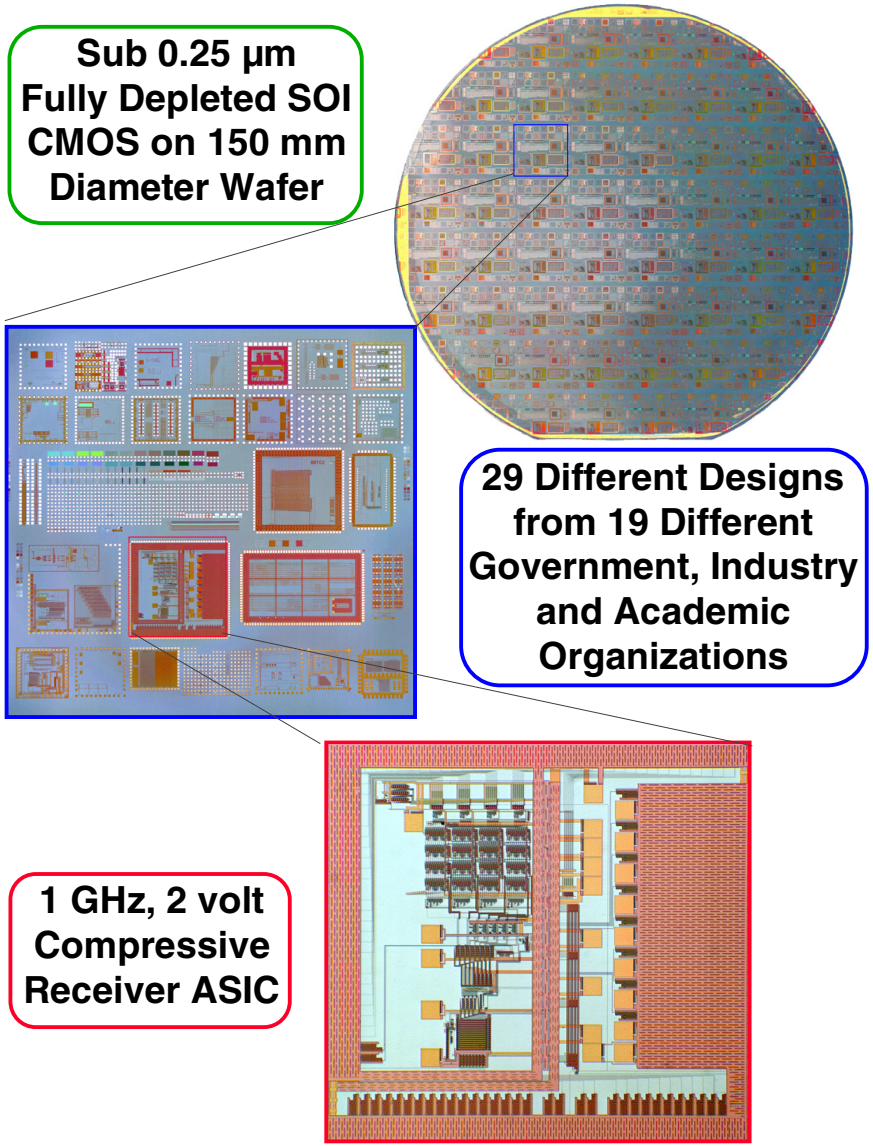
FDSOI CMOS Process Cross-section



- *25 ps ring oscillator stage delay at 2 volts*
- *1.2 GHz, 2 volt digital operation*
- *5x lower power than 0.25 µm bulk CMOS process*

Multi-Project SOI Program

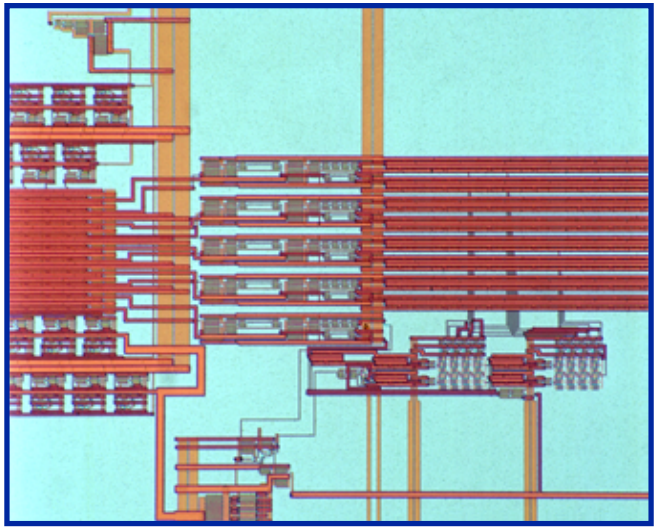
- Research prototyping for the low power/high performance circuit design community
- 92 circuits fabricated for 28 different government, industry and academic organization as part of 3 DARPA-sponsored Multiproject Runs
- Process currently transitioning from 0.25 µm to 0.18 µm design rules (MP4)
  - 0.25 µm process technology transfer to a commercial DoD fabrication facility in progress
  - DARPA-sponsored research at sub-100-nm process underway



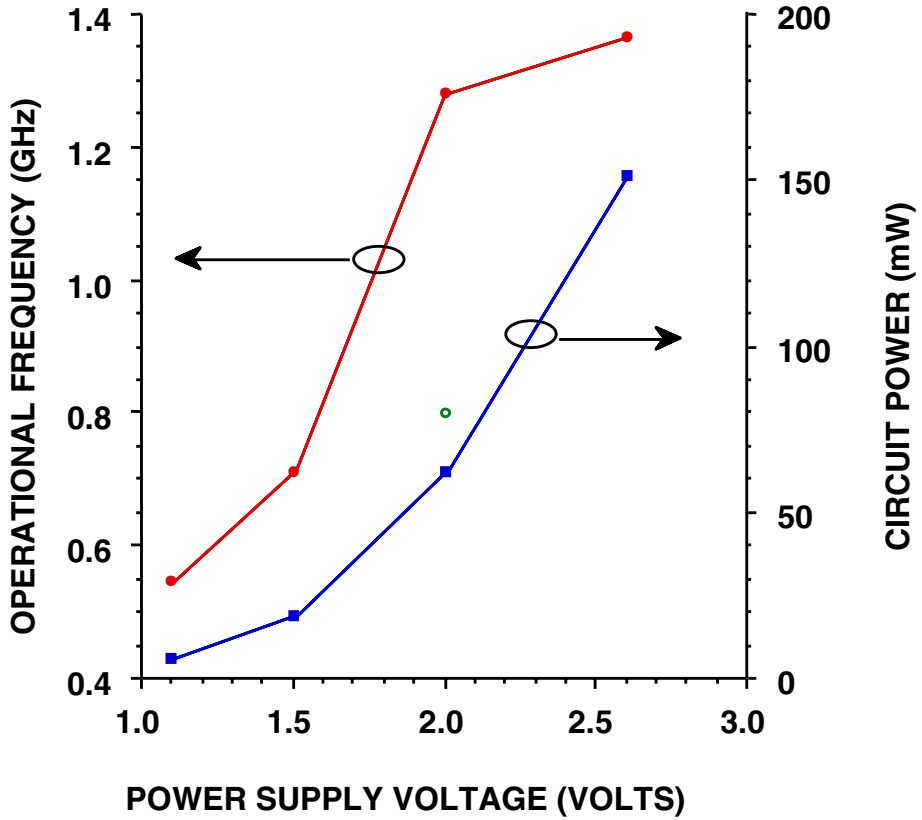
Compressive Receiver Test Chip

(0.25 µm FDSOI CMOS)

Chip Photo

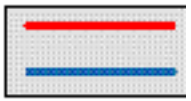


5000-Transistor Digital CMOS Circuit
Operating at 1.2 GHz, 2.0 V

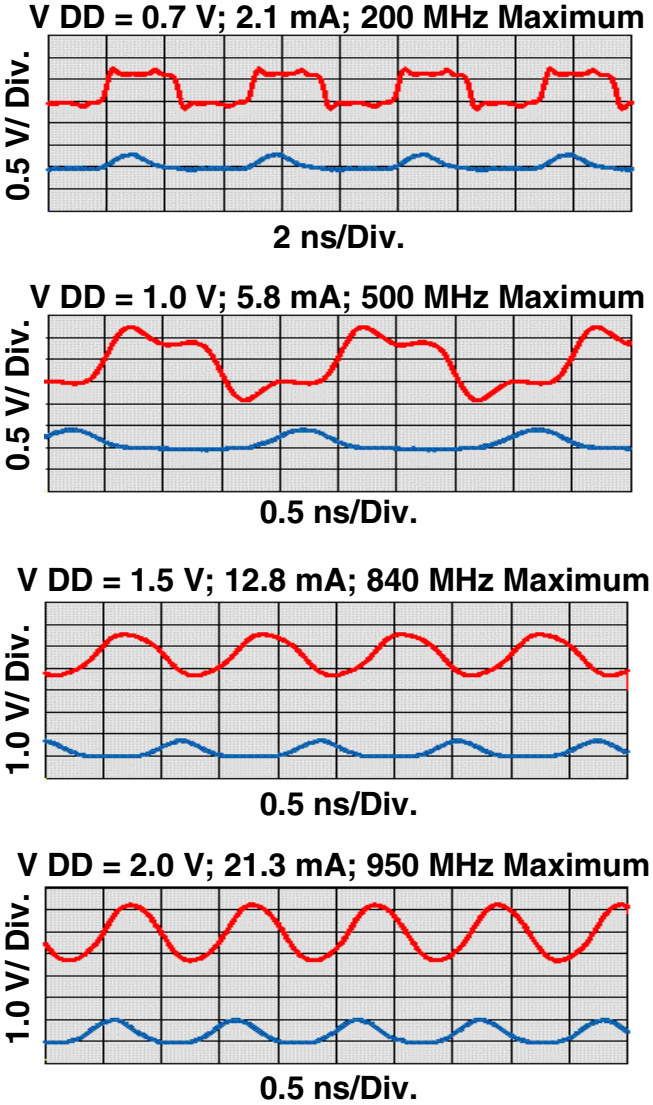


Mayo Foundation MP2 Results

- Measured results from Mayo SPPDG process benchmark test circuit
  - Fully functional data generation/acquisition circuit (DGAC) ~14,000 transistors
- Circuit is used to provide process technology benchmarking for NSA
  - 0.25 µm FDSOI CMOS technology has similar performance to Vitesse GaAs foundry (950 MHz vs. 1 GHz)
  - 0.25 µm FDSOI CMOS circuit is: 45x lower power (43 mW vs. 2 W, H-GaAs-3, measured), and 25x lower power H-GaAs-4 (simulated)



BUFIN Input
BUFOT Output



More Mayo Foundation MP2 Results

COMPARISON OF SIMULATED AND MEASURED TEST DATA FOR
NSA SYNCHRONOUS TEST SITE PLACED ON
DATA GENERATION/ACQUISITION CIRCUIT (DGAC) IMPLEMENTED IN
MIT LINCOLN LABORATORY 0.25 μm (AS-DRAWN)
FULLY-DEPLETED SILICON-ON-INSULATOR (SOI) CMOS TECHNOLOGY
(VDD = +2.0 V; Measured Data Averaged From Three Die: SN4, SN6, and SN7;
Circuits Fabricated on Multiproject Mask Set 2; HP 70841A 12 GHz Pattern Generator;
TEK 11801 Oscilloscope; 1X Picoprobes at Inputs and 10X Picoprobes at Outputs;
All Measurements Taken from Probes Directly on Die Pads)

Circuit	Input Pattern [a]	Maximum Frequency (MHz)	
		Simulated	Measured
Buffer to Buffer (DOUT1)	Divide-by-2	1200	1800
Shift Register (DOUT2)	Divide-by-2	1100	1600
	16-Bit	1000	1450
Path with 4-Bit Logic Function (DOUT3) [b]	16-Bit	1000	1000
Path with 6-Bit Logic Function (DOUT4) [c]	16-Bit	1000	1150

(a) 16-Bit Input Data Pattern = "0000001011111101"
(b) 4-Bit Logic Uses Inputs Tapped from Shift Register Path and is Placed Before Final Flip-Flop; Logic Function: A XOR B XOR C XOR D
(c) 6-Bit Logic Uses Inputs Tapped from Shift Register Path and is Placed Before Final Flip-Flop; Logic Function: ((A AND B) OR (C AND D)) XOR E XOR F

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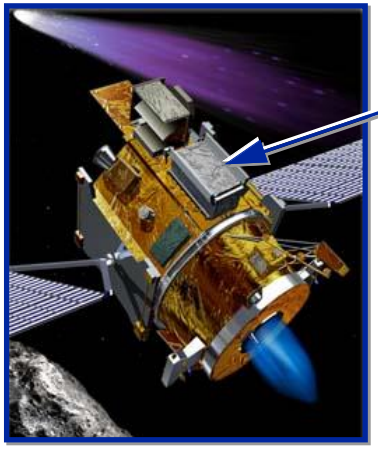
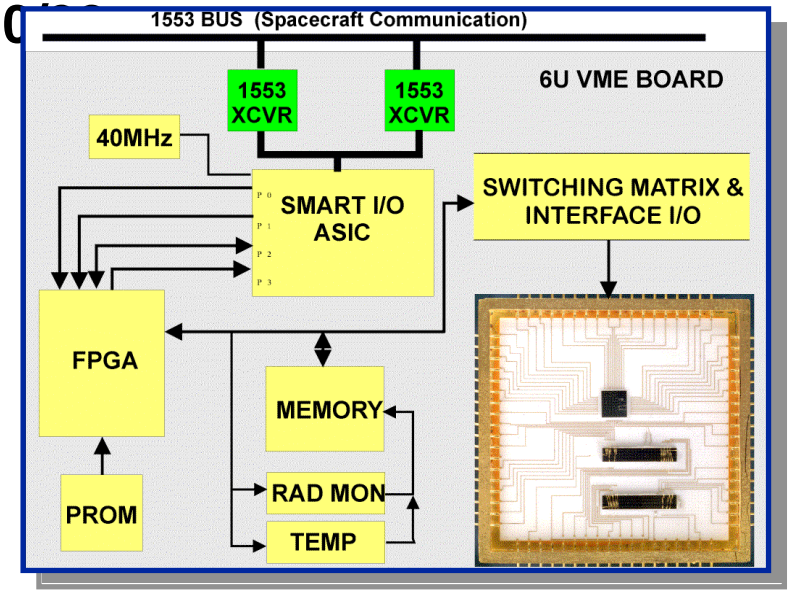
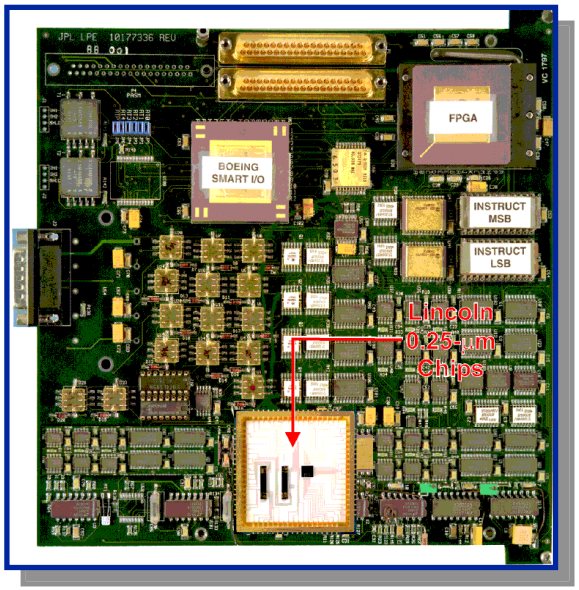
Low Power Flight Experiment

(MIT LL / NASA JPL)

- **Low power, high performance 0.25 µm FDSOI flight validation**
  - **Experimental board designed at MIT/LL**
  - **FDSOI test chips designed, fabricated and packaged at MIT Lincoln Laboratory**
- **Experiment integrated on NASA NMP Deep-Space-1 spacecraft 12/97, Launched 10/98**

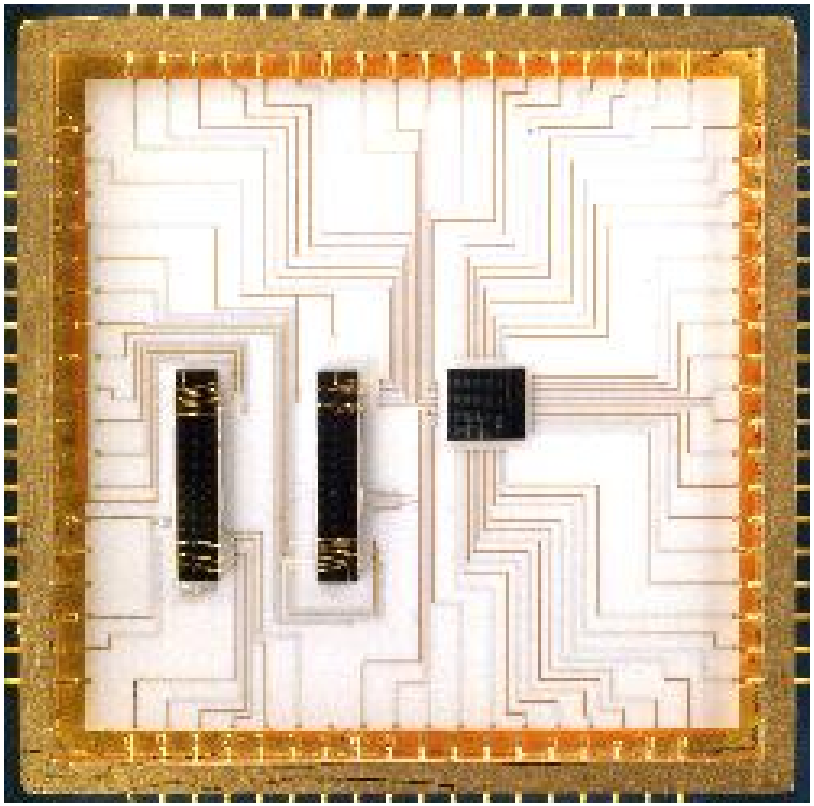






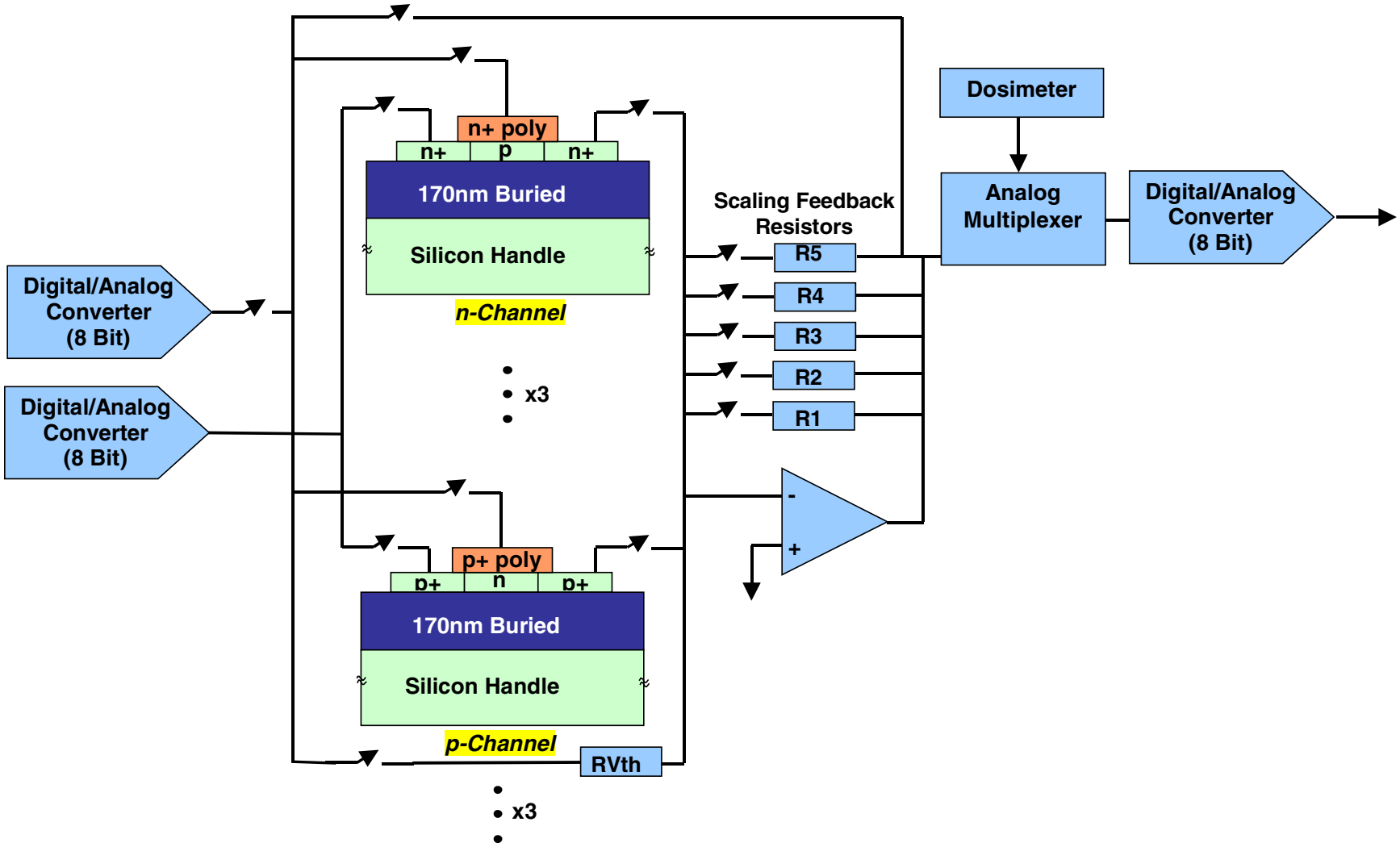
Low Power Flight Module
(Device Under Test)

- Three 0.25 μm n-channel transistors
- Three 0.25 μm p-channel transistors
- Four 97-stage ring oscillators

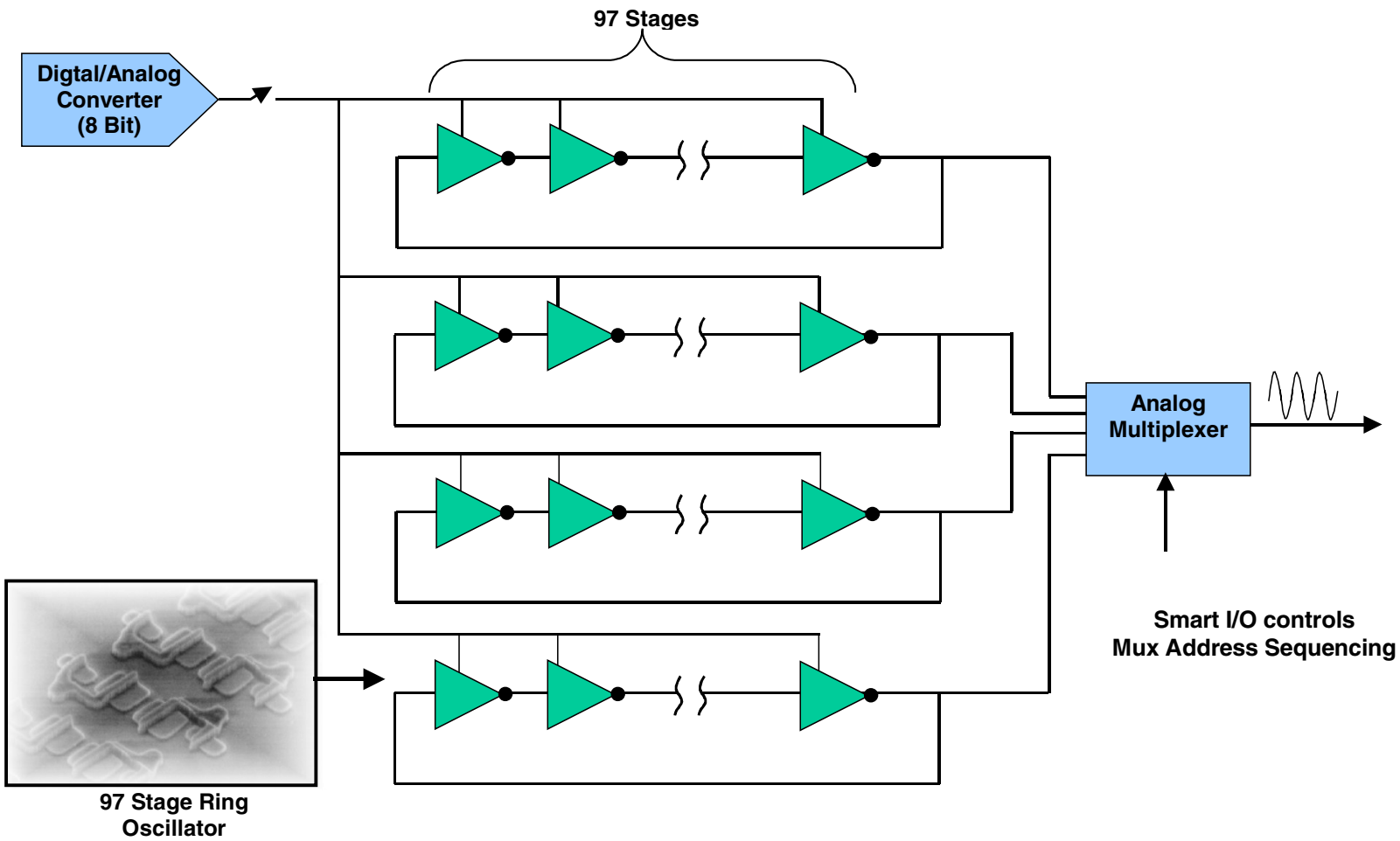


1 cm

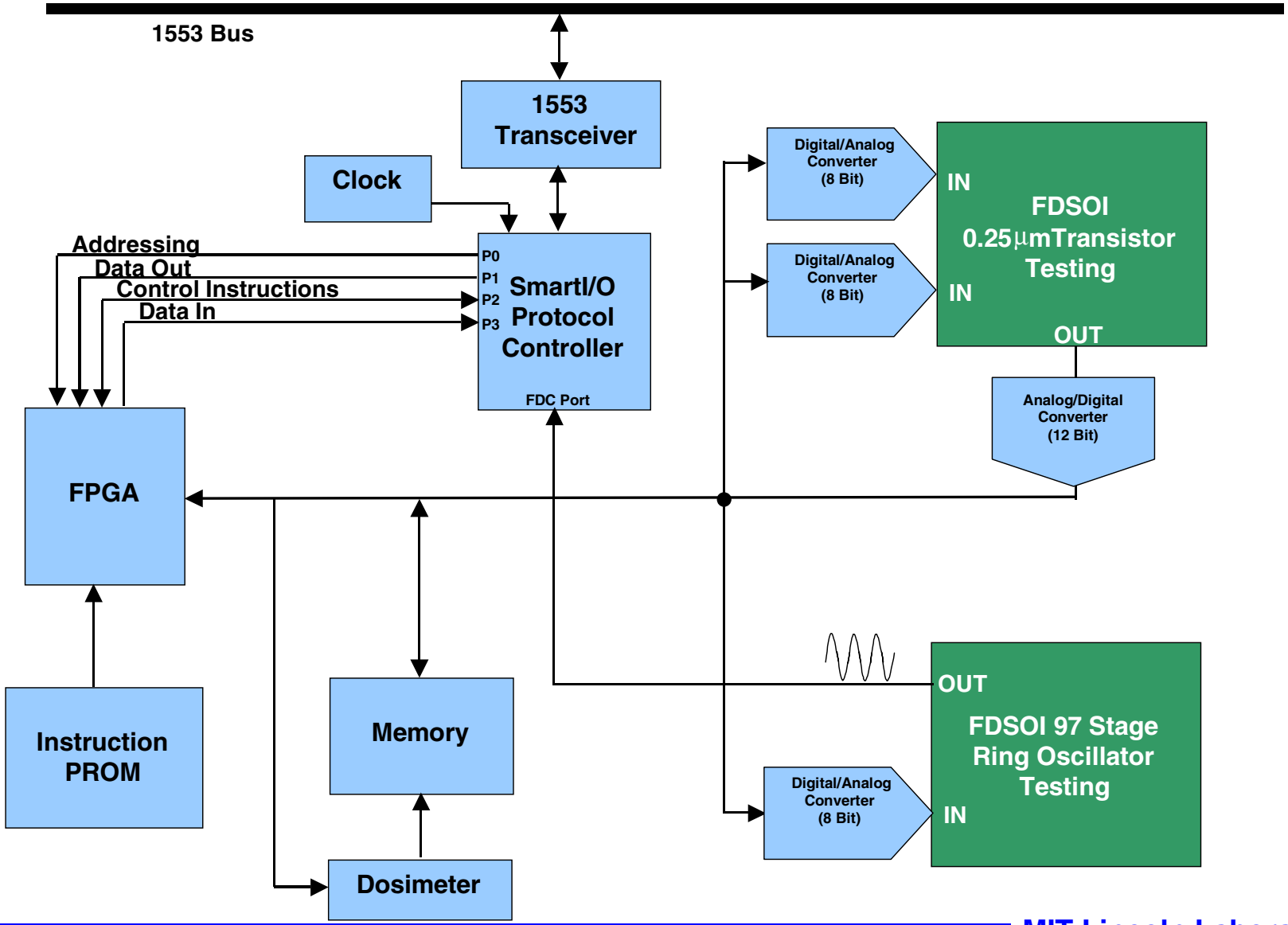
FDSOI 0.25μmTransistor Testing



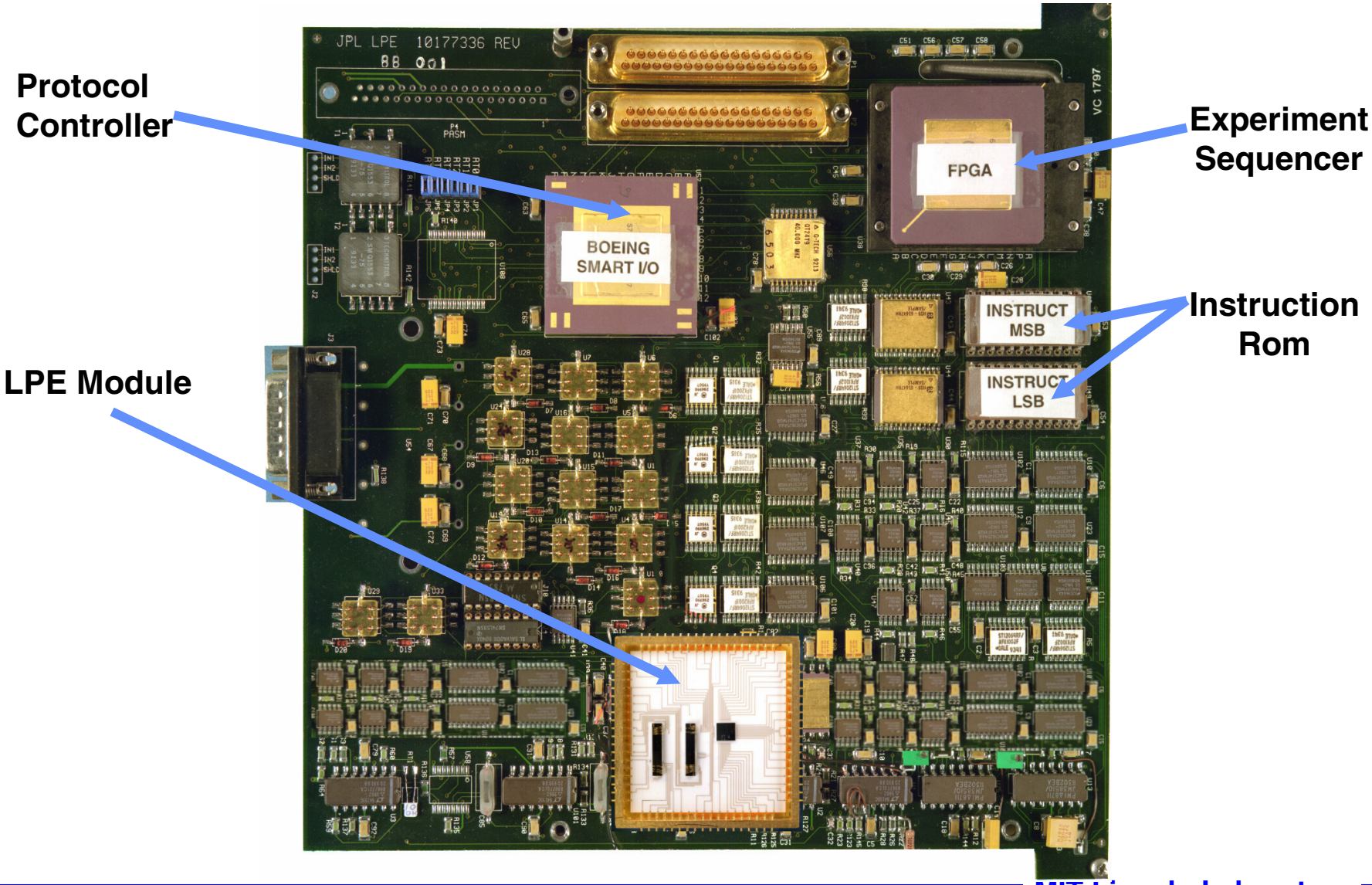
LPE 97 Stage Ring Oscillator Testing



LPE – Board Integration



LPE Board (Prototype)



8.0/0.25μm Nch Transistor Data

Test Description	*Ground Data 12/18/97	Ground Data 12/18/97	Ground Data 11/17/97	Flight Data Max Deviation From *Ground Data
Threshold Voltage	220mV	228mV	228mV	228mV
Drain-Source Leakage (Vds = 1.0V, Vgs = 0.0V)	415nA	415nA	317nA	464nA
Drain-Source Leakage (Vds = 2.0V, Vgs = 0.0V)	7.1uA	7.35uA	4.65uA	7.35uA
Drain-Source Leakage (Vds = 2.0V, Vgs = -0.5V)	13.4nA	11.2nA	11.9nA	3.2nA
Drive Current (Vds = 1.0V, Vgs = 1.0V)	1.0mA	1.08mA	1.07mA	1.08mA
Drive Current (Vds = 2.0V, Vgs = 2.0V)	2.9mA	2.9mA	2.9mA	2.9mA
Saturation Transconductance gmSat	123uS	122uS	145uS	148uS
Drain-Source Output Conductance Gds	1555uS	1557uS	1684uS	1531uS

* Last ground test before launch

A/D Converter Resolution = 2mV/Count

8.0/0.25μm Pch Transistor Data

Test Description	*Ground Data 12/18/97	Ground Data 12/18/97	Ground Data 11/17/97	Flight Data Max Deviation From *Ground Data
Threshold Voltage	-299mV	-326mV	-306mV	-316mV
Drain-Source Leakage (Vds = -1.0V, Vgs = 0.0V)	2.4nA	2.4nA	2.4nA	2.4nA
Drain-Source Leakage (Vds = -2.0V, Vgs = 0.0V)	24nA	24nA	73nA	24nA
Drain-Source Leakage (Vds = -2.0V, Vgs = 0.5V)	6.1nA	5.6nA	7.2nA	5.6nA
Drive Current (Vds = -1.0V, Vgs = -1.0V)	339uA	341uA	326uA	321uA
Drive Current (Vds = -2.0V, Vgs = -2.0V)	1.2mA	1.2mA	1.2mA	1.2mA
Saturation Transconductance gmSat	99uS	99uS	98uS	99uS
Drain-Source Output Conductance Gds	790uS	841uS	781uS	786uS

* Last ground test before launch

A/D Converter Resolution = 2mV/Count

Ring Oscillator Data

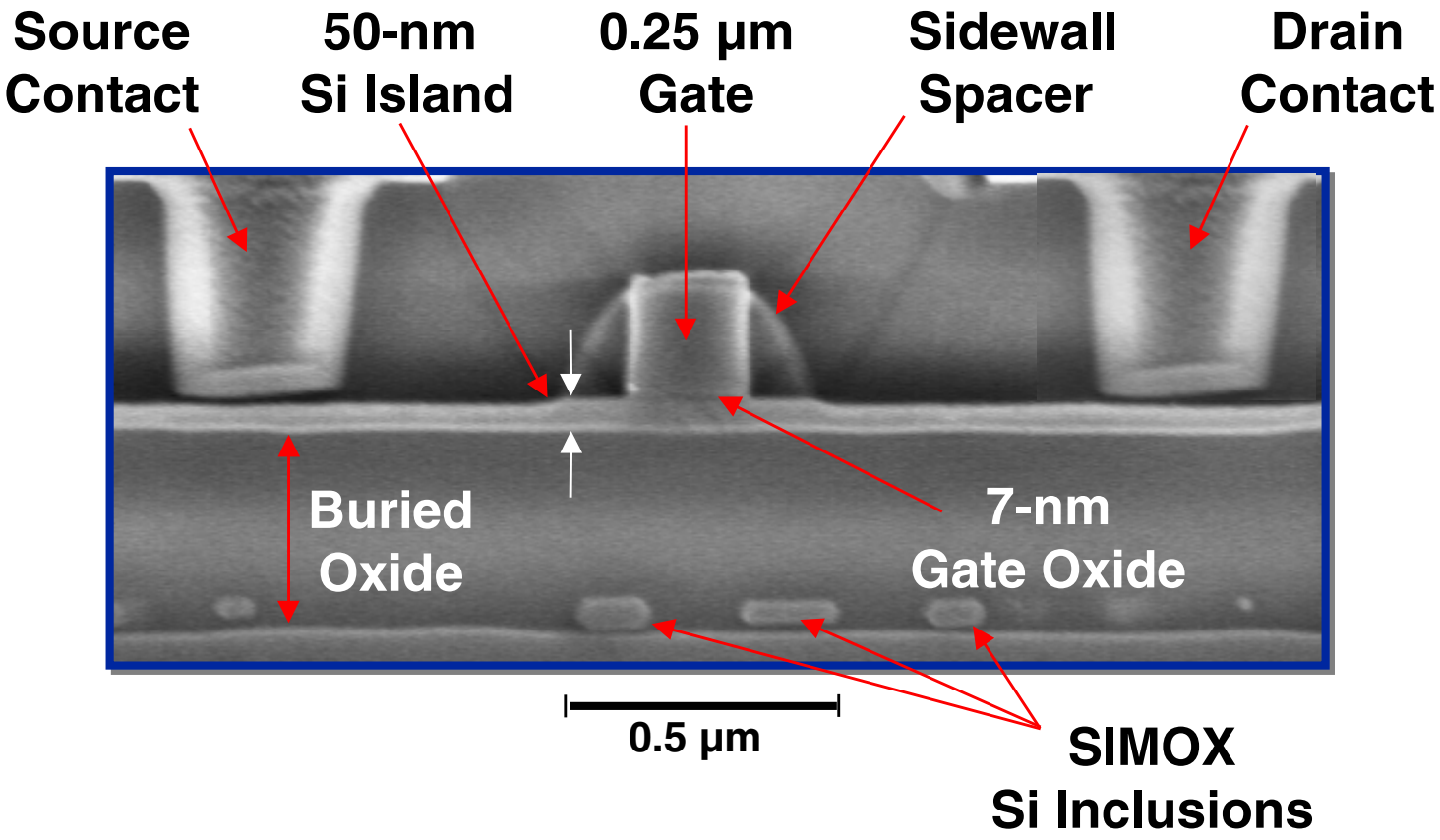
Test Description	*Ground Data 12/18/97	Ground Data 12/18/97	Ground Data 11/17/97	Flight Data Max Deviation From *Ground Data
Ring Oscillator #1 Delay/Stage	40.7ps	41.5ps	41.2ps	41.6ps
Ring Oscillator #2 Delay/Stage	41.2ps	40.9ps	40.6ps	42.3ps
Ring Oscillator #3 Delay/Stage	41.7ps	40.5ps	40.2ps	42.8ps
Ring Oscillator #4 Delay/Stage	43.1ps	39.17ps	38.8ps	44.4ps

Preliminary Radiation Performance Total Dose

- Note: Initial process developed for low power, high performance operation, no effort was made to optimize radiation performance
- Radiation testing was done on an ARACOR Model 4100 Semiconductor Irradiation System with an X-ray source
  - Dose rate was10k rad(Si) per minute for 0-200k rad and 130k rad(Si) per minute 200k-1000k rad
  - Device was biased with 1 volt on the gate and 0 volts on the source, drain, and substrate

    "Pass gate" bias was 1 volt on the drain, 0 volts on the source, gate and substrate
  - Devices were measured immediately after irradiation

FDSOI Transistor Cross Section

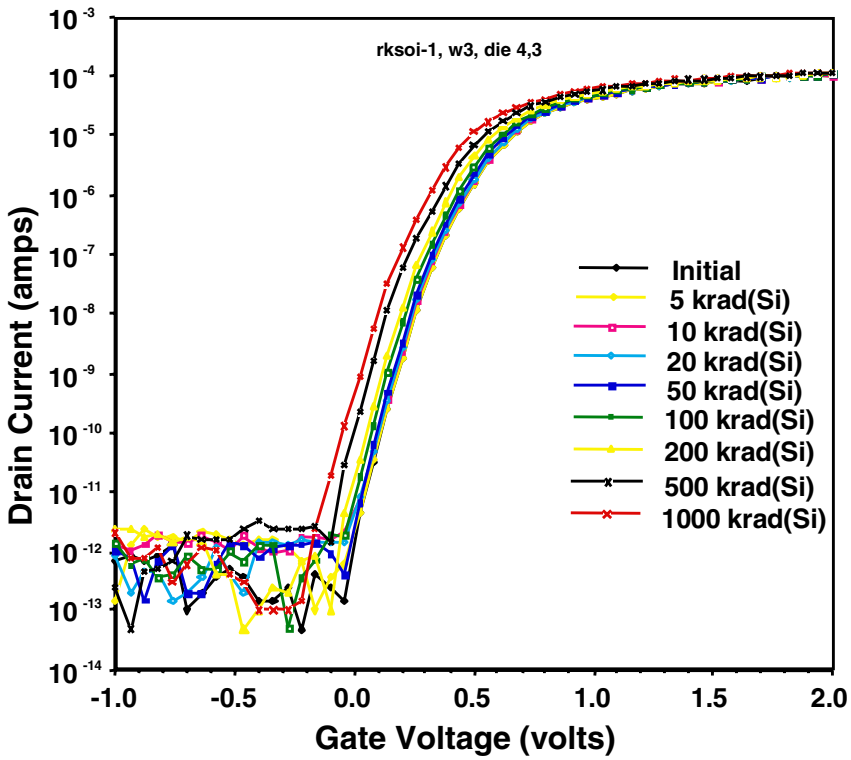


Low Power SOI Radiation Performance

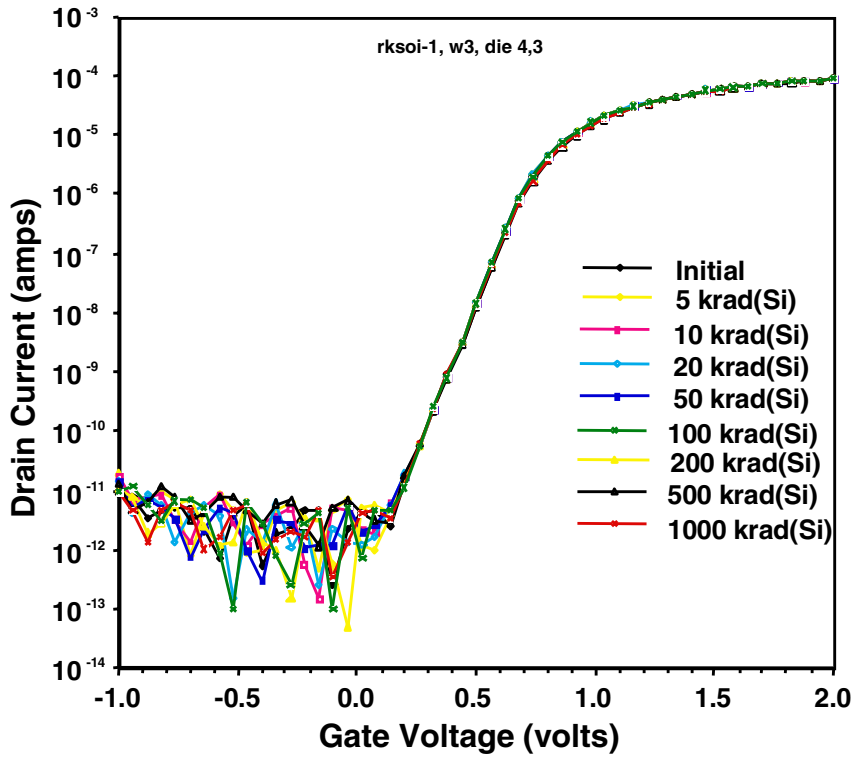
(Bias, $V_{ds}=V_{sb}=V_{bs}$ = 0 volt, V_{gs} = 1 volt)

(n-channel, W/L = 8.0 µm / 0.25 µm)

Wafer Voltage = 0 volts

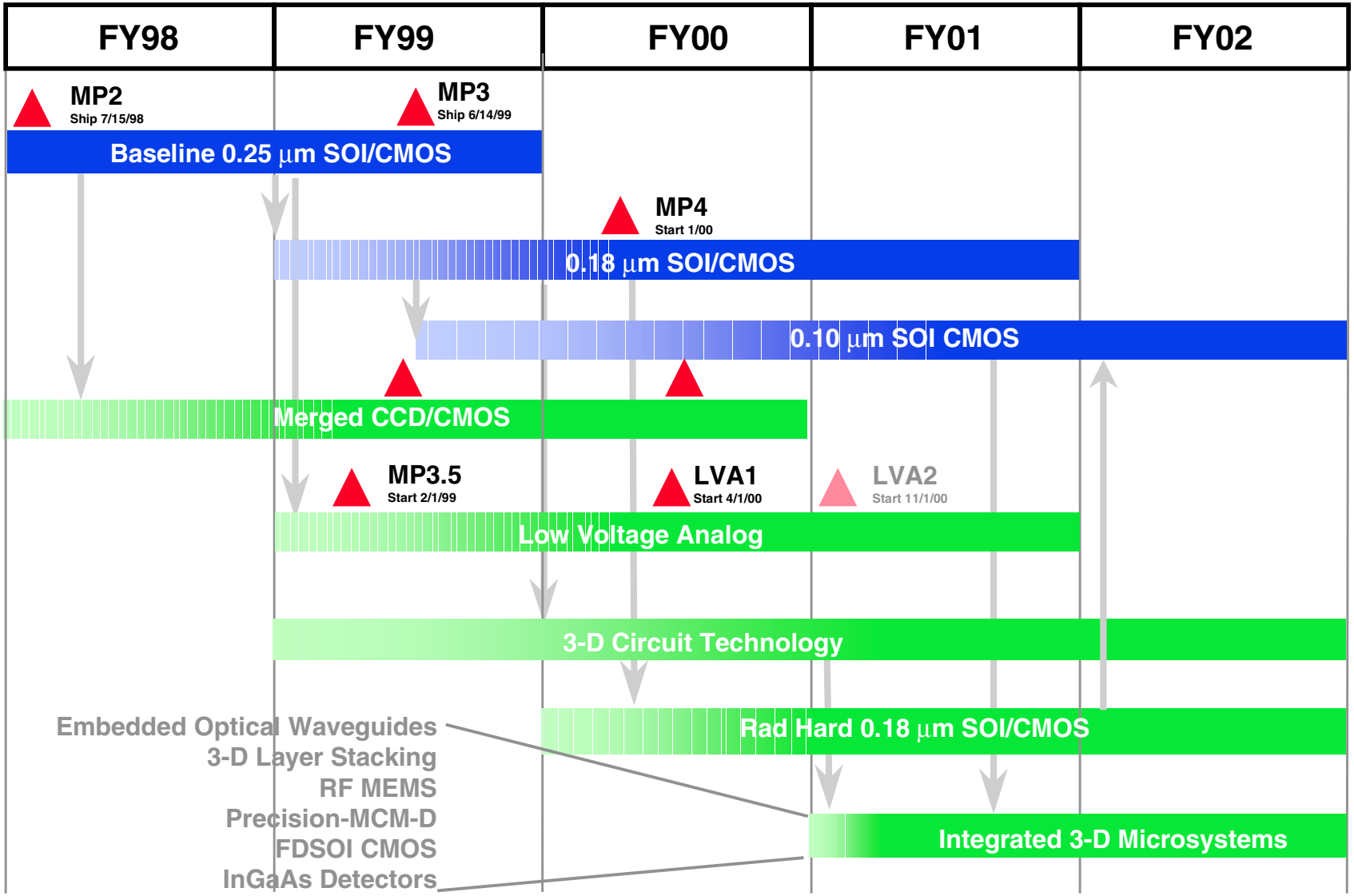


Wafer Voltage = -30 volts

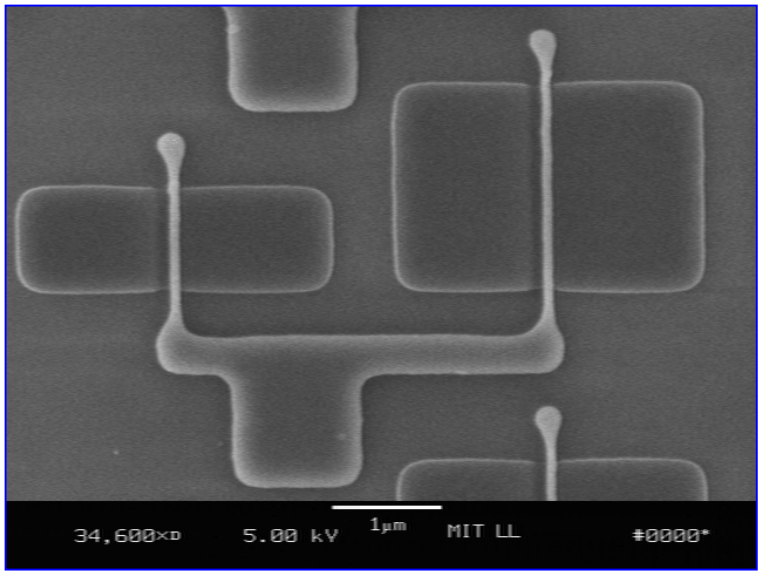


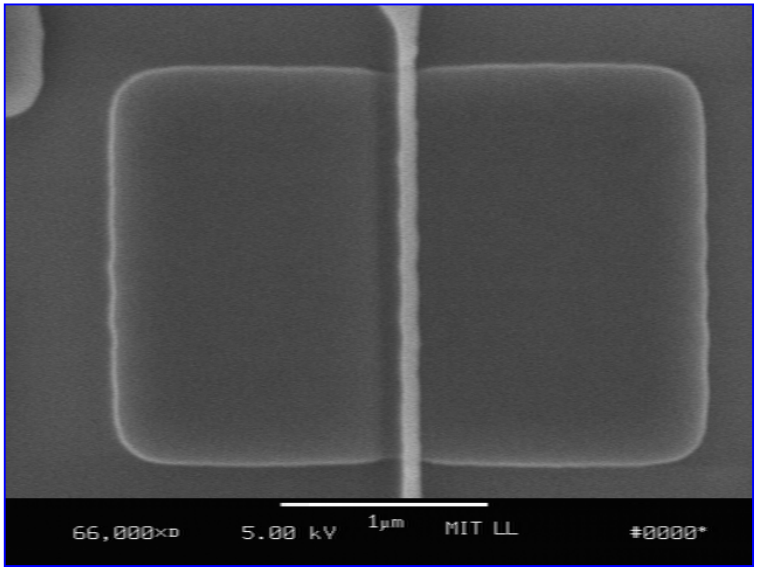
~140 mV threshold shift at 1 Mrad(Si)

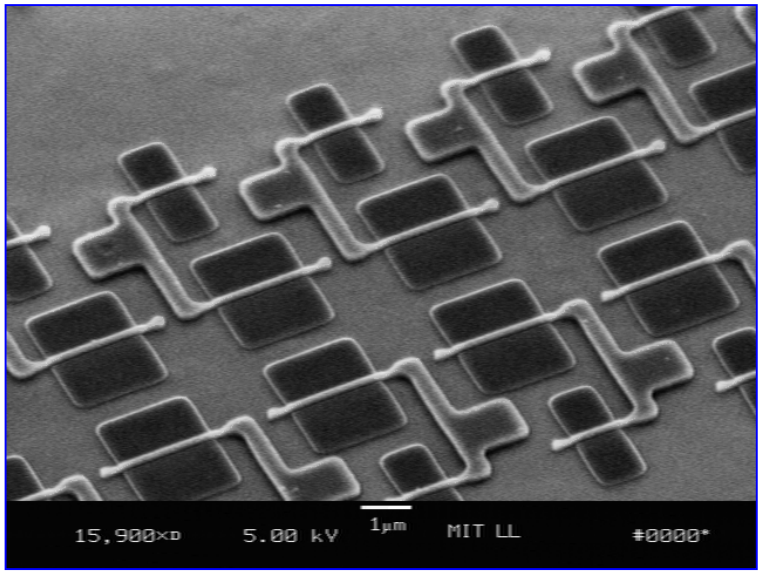
Low Power, High Performance FDSOI CMOS Roadmap

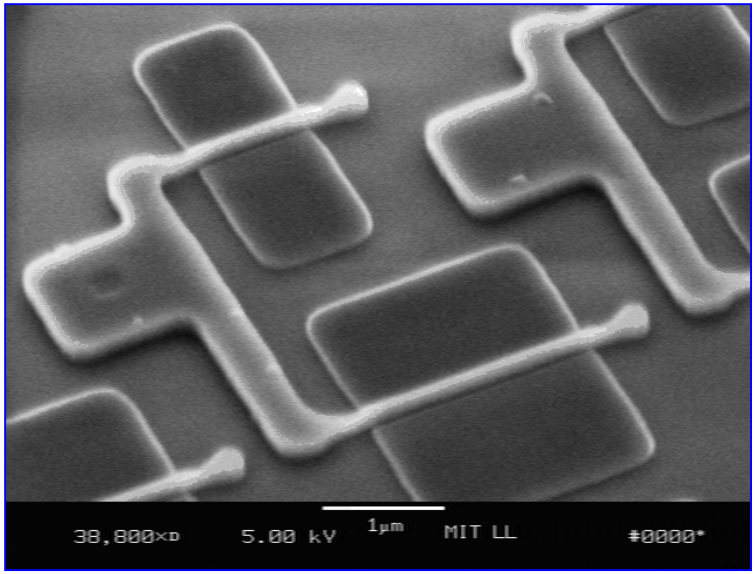


Sub-100-nm FDSOI CMOS Development
(83 nm Gate Length Inverters)





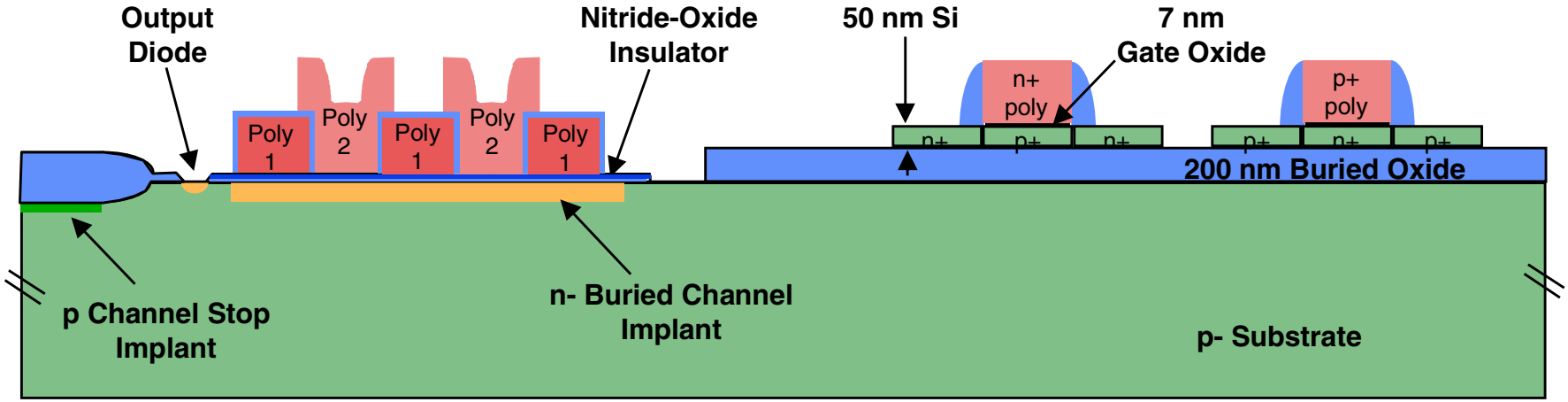


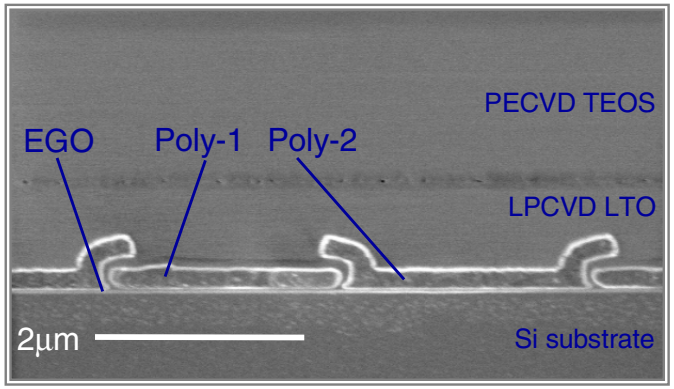


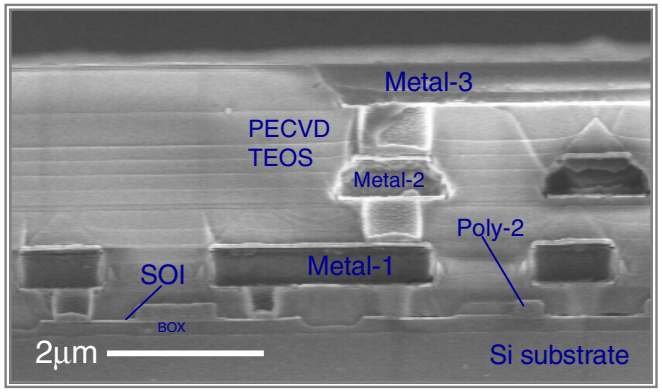
FDSOI Process Extensions
Integrated CCD/SOI CMOS Process

4-phase, buried channel CCD

Fully depleted SOI CMOS

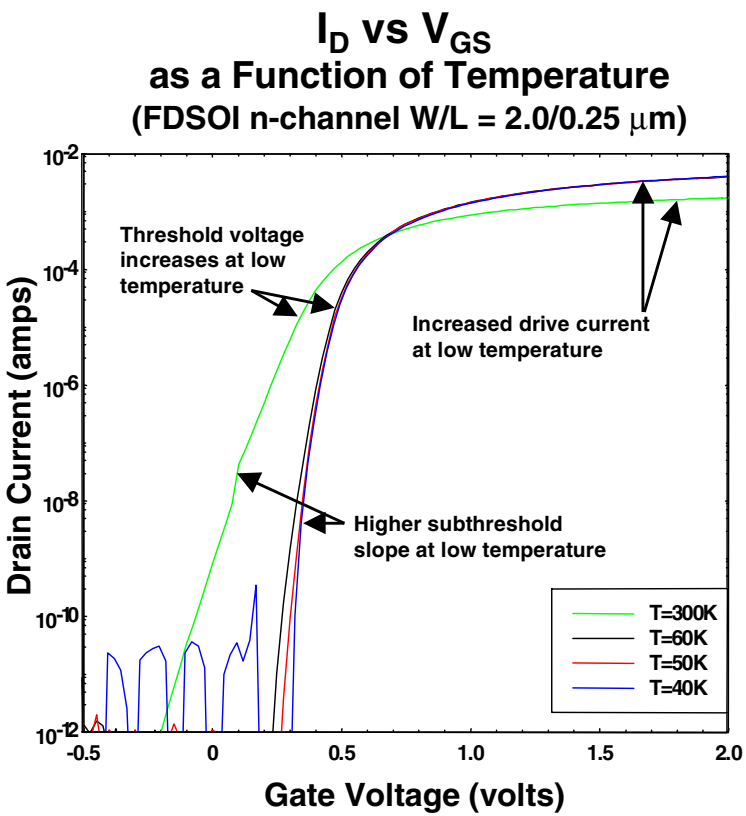




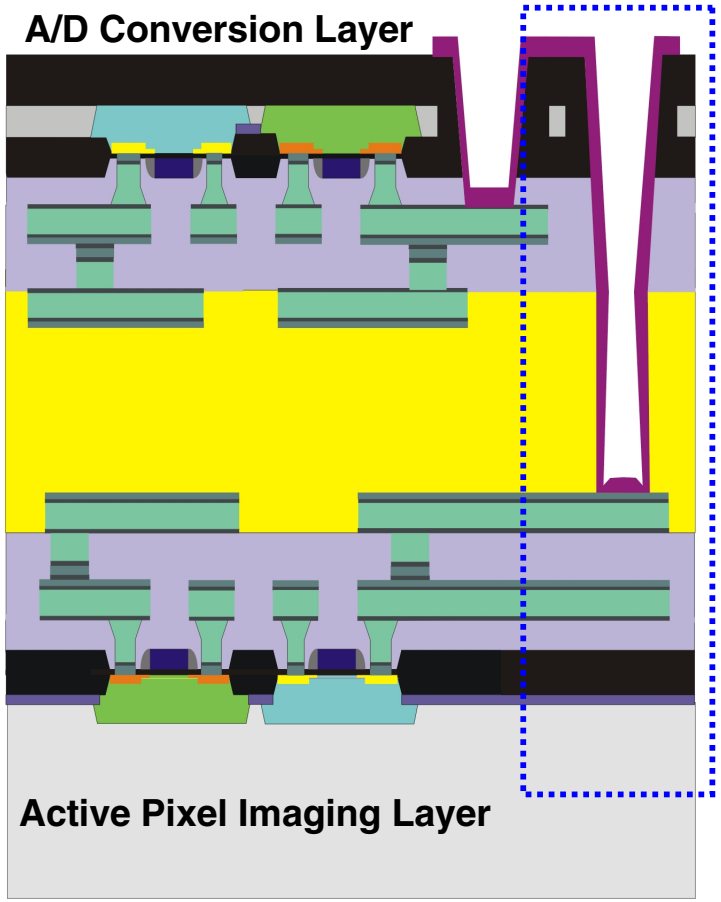


FDSOI Process Extensions
Low Voltage Analog

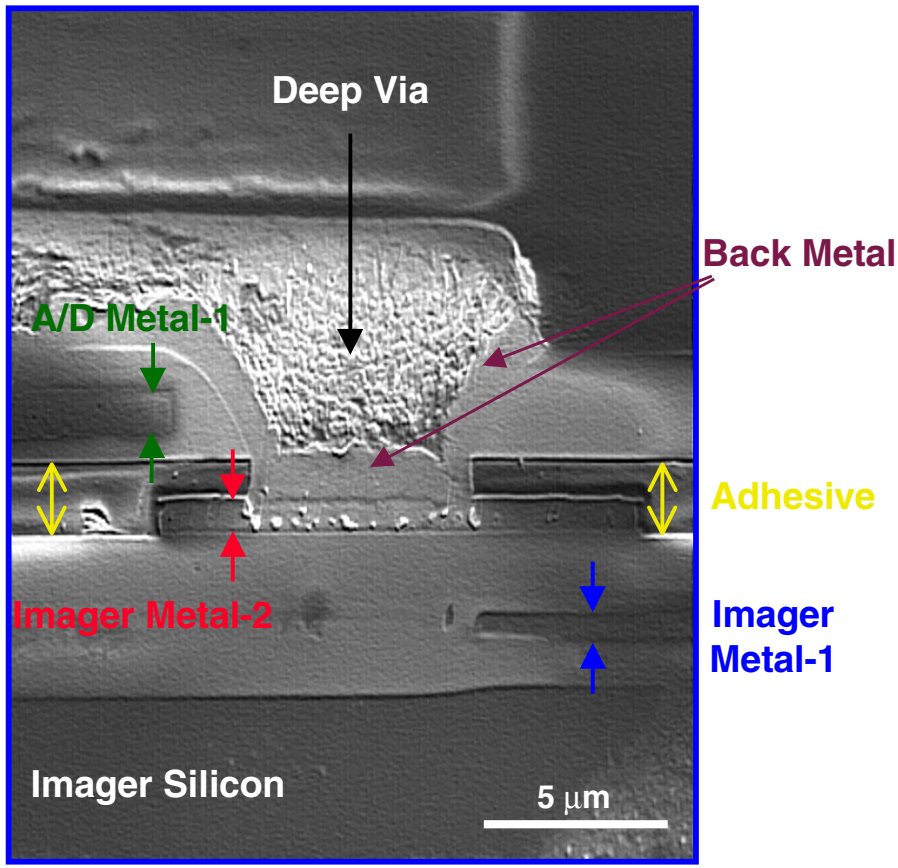
- Investigate the feasibility of fabricating ultra-low power analog circuits in MIT Lincoln Laboratory's 0.25 µm, 2 volt, fully depleted silicon-on-insulator (FDSOI) CMOS process technology
  - Analog test device design and cryogenic characterization
- Integrate low voltage and temperature coefficient capacitors into the baseline technology
- Generate SOI-SPICE models and design rules for the low voltage analog technology
- Integrate designs onto a common reticle set and fabricate a dedicated low voltage analog multiproject run



FDSOI Process Extensions
3-D Integration Using SOI



Deep Via Cross Sectional SEM



Summary

- Reviewed the sub-0.25-µm fully depleted SOI CMOS technology undergoing deep space validation
  - 5x lower power than 0.25 µm bulk CMOS technology
  - > 1GHz operation at 2 volts, 43 GHz n-channel f_T
- Described the design of the Low Power Flight Experiment
  - Experiment data indicates essentially no change in device performance during launch and space flight
  - Potential for successful operation in extreme total dose environments
- Showed some process extensions and future directions of the FDSOI technology